Mrs. Y. Sudha Vani

Associate Professor

Department

Electronics and Communications Engineering

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Academic Background

Pursuing P.hd. (Low Power VLSI) - Vignan's (VFSTR) University.

M.Tech (VLSI system design) – Gokaraju Rangaraju Institute of Engineering and Technology, JNTU of Hyderabad

B.Tech (ECE) – Loyola Institute of Technology and Management

Mrs. Y Sudha Vani has rich experience in the field of Low power VLSI. She has taken subjects related to VLSI and has been proficient in teaching subjects like Digital Electronics, Digital IC Applications, Verilog HDL, and VLSI design.

She has published 8 papers in various journals and conferences which are indexed in Scopus and Science Citation Indexing.

Research Interests:

Low power VLSI, Magnetic Memories, Arithmetic computing, In-memory computing, Neuron computing.

Achievements:

Acting as a reviewer of international journal of electronics

A paper titled "" Carbon Nano Tube Field Effect Transistors Based Ternary Ex-OR and Ex-NOR Gates" ***Current Nanoscience, 2016*** (SCI Indexed Journal)

A paper titled "" Low Write Energy STT-MRAM Cell Using 2T-Hybrid Tunnel FETs Exploiting the Steep Slope and Ambipolar Characteristics" *Springer nature , 2017* (Scoups indexed Journal)

A paper titled "A 128Kb RAM Design with Capacitor-Based Offset Compensation and Double-Diode based Read Assist Circuits at Low V_{DD}" **Journal of Scientific and Industrial Research (JSIR)** Sep 2020 (SCI Indexed Journal)

A paper titled "An Energy-Efficient Hybrid Tunnel FET based STT-MRAM memory cell at Low V_{DD}" **international journal of electronics, 2021** (SCI Indexed Journal).