

**Mr. Pyla Rajesh**

Assistant Professor

**Department**

ECE

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**Academic Background:**

M.Tech (VLSI Design)–MVGR College of Engineering

B.Tech (ECE)–Raghu Engineering College

Mr. Pyla Rajesh has rich experience in the field of VLSI. He has taken subjects related to Digital Electronics and has been proficient in teaching subjects like DE, LICA, DICA, Analog and Digital Communications.

He has published 9 papers in various International Journals which are UGC Approved.

**Research Interests:**

Low Power VSLI  
Mixed Signal VLSI Design

**Achievements:**

- **Qualified UGC NET for Lectureship in the year 2013**
- Published paper on, “A 3GHz Low-offset Fully Dynamic Latched Comparator for High-Speed and Low-Power ADCs”, IJETAE, pp. 96-102, Volume 3, Issue 6, June 2013.
- Published paper on, “An Area Efficient Low Power Fully Dynamic Latched Comparator in Nano Scale Technologies”, IJECT, pp. 96-99, Volume 4 Issue 3, July-Sep 2013.
- Published paper on, “An Area Efficient Low Power High Speed Pulse Triggered Flip Flop Using Pass Transistor”, IJSCE, Volume-5 Issue-2, Page No.: 37-40, May 2015.
- Published paper on, “Comparative Performance Analysis of Low Power Full Adder Design in Different Logics in 22nm Scaling Technology”, (IJCI) Vol. 5, No. 4, August 2016.

- Published paper on, “An Optimized Low-Voltage Low-Power Double Tail Comparator for High-Speed ADCs”, IJAET, Volume 9 Issue 3- June 2016.
- Published paper on, “Comparative Analysis of Pulsed Latch and Flip-Flop based Shift Registers for High-Performance and Low-Power Systems”, IJECT Vol. 7, Issue 2, April - June 2016.
- Published paper on, “Full Adder Designs Using Low Power Full Swing Xor and Xnor Structures” IJITEE, Volume-8 Issue-8 June, 2019(**Scopus Indexed**)
- Published paper on, “Low Power GDI Full Swing Full Adder Design For Area and Energy-Efficient DSP Systems”, JECA, Volume 10, Issue 6, June/2020
- Published paper on, “Low Power GDI Based Full Swing Multiplier Design For Energy-Efficient DSP Systems”, JASC, Volume VII, Issue VI, June/2020.